**Module 8: Timer, GPIO and 7-Segment Peripherals**

1. Which of the following tasks is typically performed by a timer peripheral?

1. Managing the data flow between a system bus (e.g., AHB) and a monitor
2. Transforming data from serial to parallel
3. Generating interrupt signals
4. Providing temporary storage space

2. Which of the following tasks is typically performed by a GPIO peripheral?

1. Providing an interface between the system bus and an LCD screen
2. Generating variable width pulses
3. Providing additional storage space for data and control signals
4. None of the above.

3. Which of the following tasks is typically performed by a 7-segment peripheral?

1. Providing an interface between the system bus and an LCD screen
2. Performing frequency division
3. Providing additional storage space for data and control signals
4. None of the above.

4. Which of the following is a task of the compare register used in the timer peripheral architecture?

1. Generating interrupt signals
2. Providing a temporary storage space
3. Converting data from parallel to serial
4. Continuously comparing the data value stored in the timer register and that stored in the capture register

5. A timer peripheral is designed with the following specifications: the register timer counts from 0 to 199 and then rests itself. The compare register is preloaded with a value of 20. Assuming the timer is running in the PMW mode, what is the duty cycle of its output signal?

1. 50%
2. 25%
3. 20%
4. 10%

6. Which of the following factors should be considered when designing the frequency division block in the 7-segment display peripheral?

1. The clock speed of the host system
2. The sensitivity of the human eye to variations of colors
3. The latency of the anode decoder
4. All of the above.

7. What is the minimum number of wires needed at the output of the address decoder in the 7-segments display peripheral architecture?

1. 3
2. 4
3. 2
4. 1

8. Which of the following factors have an impact on the timing precision of a hardware timer? (There may be more than one correct answer.)

1. The clocking speed of the host system
2. The design of the prescaler
3. The data value pre-loaded to the compare register
4. The latency of the AHB bus interface

9. Which of the following statements is an advantage of hardware timer over a software timer? (There may be more than one correct answer.)

1. It saves the microcontroller’s time.
2. Its area overhead is smaller.
3. It reduces power consumption.
4. It offers a high level of time precision.

10. Why are GPIO peripherals widely used in systems on chips? (There may be more than one correct answer.)

1. To facilitate the interaction between the system and the environment, especially in embedded applications
2. To facilitate the integration of IP cores from different vendors to achieve required functionality
3. To interface with the system bus
4. To improve the performance of the system by enhancing its storage capacity